AMENDMENTS TO THE SPECIFICATIONS:

Please amend the paragraph beginning on page 1, line 19 and ending on page 2, line 3, as follows:

-- Many different types of physical phenomena may be modeled using numerical simulations. In the field of aerospace engineering, for example, numerical simulations are widely used to predict a variety of phenomena, including airflow over aerodynamic surfaces, electromagnetic scattering from reflective bodies, and mechanical stresses within structures. Examples of computational simulations also may be found in the fields of medical research, electrical engineering, geology, atmospheric sciences, and many other scientific fields. Such simulations may provide valuable information that may otherwise be very difficult and very expensive to determine experimentally. This is particularly true for models which include a large number of operations which would normally be performed in a parallel fashion in the real world but must be performed in serial fashion in the computer model due to a limited number of Central Processing Units (CPU's). --

Please amend the paragraph beginning on page 3, line 1 and ending on page 4, line 3, as follows:

-- FIGURE 4 is a schematic view of the Very High Speed Integrated Circuit Hardware Description Language (VHDL) Synthesis process which is unique part of a hardware-based method for performing simulations in accordance with an embodiment of the present invention.--

Please amend the paragraph beginning on page 4, line 13 and ending on page 4, line 22, as follows:

-- Apparatus and methods in accordance with the present invention may use programmable devices, such as high density Field Programmable Gate Array (FPGA) chips mounted in PC cards, to run a hardware portion of the simulation. Prior art uses of FPGA chips

utilize only a one way path for the circuit design under development and do not include a data path between a running simulation and the portions resident on the programmable device (*e.g.* FPGA). Apparatus and methods in accordance with the present invention, however, provide function blocks which allow a user to develop simulations which can have all or some of the blocks running in a programmable hardware module (*e.g.* an FPGA) instead of the serial CPU in the computer and maintain the flow of data and control as if the simulation were running in a high speed simulation. --

Please amend the paragraph beginning on page 5, line 3 and ending on page 5, line 15, as follows:

-- In one embodiment, the programmable module 218 may be a field programmable gate array (FPGA) chip. Alternately, the programmable module 218 may be a Digital Signal Processing (DSP) chip, such as the DSP chips of the type generally offered by Texas Instruments, Incorporated of Dallas, Texas, or Analog Devices, Inc. of Norwood, Massachusetts. In one particular embodiment, the Peripheral Component Interconnect (PCI) bus card 218 may be a Bennuey card of the type commercially-available from Nallatech, Inc. of Orlando, Florida, having a 3 million gate FPGA chip manufactured by Xilinx, Inc. of San Jose, California. The hardware-based method 200 may be provided with a software package that enables the interface module 216 to generate the internal programming code that operates in conjunction with the other components of the method 200. For example, in one particular embodiment of the method 200, it is equipped with the System Generator software available from Xilinx, Inc. that generates VHDL code that operates in conjunction with the above-referenced SIMULINK modeling software. --

Please amend the paragraph beginning on page 6, line 3 and ending on page 6, line 10, as follows:

-- As further shown in FIGURE 2, the output is coupled to a gateway out block 236 that is adapted to convert fixed point data to double precision data, and may also serve as an output point for a top level Hardware Description Language (HDL) design. The outputs of the gateway out blocks 236 are coupled to a second input of the PCI bus card 216, which in turn has a second output leading to a scope 238 for analyzing results. Using the simulation results displayed on the scope 238, the scientist or engineer may make further decisions regarding, for example, the design of the reflective body, or the design of the radar system that generates incident electromagnetic signals. --

Please amend the paragraph beginning on page 6, line 16 and ending on page 7, line 4, as follows:

-- FIGURE 3 is a schematic view of the development process for the hardware-based method 200 of FIGURE 2. In this embodiment, the method 300 includes modeling a design for simulation using, for example, a prior art design tool (*e.g.* SIMULINK, etc.) in a block 200. In a block 304, the VHDL blocks that form the hardware-based method 200 (*e.g.* blocks 220 through 236) are generated. In one particular embodiment, the VHDL blocks may be formed using a System Generator software package 305 available from Xilinx. In a block 306, a synthesizeable VHDL code is generated. This VHDL provides the hardware description of the circuits necessary to implement the Simulink diagram functionality. If the specific implementation requires more than one portion of the simulation to be placed in hardware there will be a corresponding number of VHDL files generated. In a block 308, a VHDL simulator can be used to verify the performance of the generated VHDL before further work on the simulation is performed. Once the developer is sure that the generated VHDL code is accurately performing it's function, synthesis of the hardware programming BIT file may proceed. VHDL synthesis is performed in block 310. The end product of the VHDL generation process is a combined VHDL file that specifies all of the hardware to be programmed into the FPGA chip. This file is synthesized into a BIT file which is used to program the gate connections of the FPGA chip to

accurately model the circuit diagram being designed. Then, in a block 312, a device is programmed using a Binary Digit (BIT) file from the VHDL synthesis of block 310. --

Please amend the paragraph beginning on page 7, line 5 and ending on page 7, line 17, as follows:

-- FIGURE 4 is a schematic view of the VHDL Synthesis process. The top level VHDL synthesis 410 includes a communication core block 412 that provides communication between the programmable module 402 and a user developed controller 414 via a register interface 416. A DMA interface 418 of the communication core block 412 is coupled to a user developed interface to the generated VHDL code block. In this embodiment an input First-In-First-Out (FIFO) buffer 420 leading to a VHDL code block 422, and to an output FIFO buffer 424 leading from the VHDL code block 422. The VHDL code block 422 may be any suitable type of VHDL code, including, for example, those VHDL cores accessed from libraries of tested circuits, the System Generator output from Xilinx, and any other suitable VHDL generators, including user-created VHDL code. The various blocks of VHDL code are combined into a single VHDL file for each of the programmable devices. The combined VHDL file is then processed by hardware specific synthesis code, such as Xilinx Synthesis Technology (XST), which produces the hardware configuration BIT File. --